In the Claims:

1. (Original) An integrated circuit device, comprising:

an integrated circuit chip having a clock driver therein that supports generation of a plurality of output clock signals having different frequencies in a range between 1 and 1/N times a frequency of an internal clock signal and full-period programmable skew characteristics, where N is a positive integer greater than one.

2. (Original) The integrated circuit device of Claim 1, wherein the clock driver comprises an internal clock signal generator selected from the group consisting of a phase-locked loop (PLL) integrated circuit and a delay-locked loop (DLL) integrated circuit.

3. (Original) The integrated circuit device of Claim 2, wherein the clock driver is configured to support generation of a divide-by-N clock signal having a full-period programmable skew characteristics that is stepped in NxM time units having a duration equal to 1/M times a period of the internal clock signal, where M is a positive integer greater than eight.

4. (Original) The integrated circuit device of Claim 3, wherein M=CxF, and C and F are positive integers; and wherein the NxM time units extend over a full-period of the divide-by-N clock signal at time points defined by: {(-((½C×N)-1)ctu, -(½F)ftu), ..., (+((½C×N)-1)ctu, +((½F)-1)ftu), (invert, -(½F)ftu)), ..., (invert, +((½F)-1)ftu)}, where "ctu" designates a coarse time unit and "ftu" designates a fine time unit.

5. (Original) The integrated circuit device of Claim 3, wherein M=CxF, and C and F are positive integers; and wherein the internal clock signal generator comprises a differential voltage-controlled oscillator having at least ½C stages therein.

6. (Currently amended) ~~The integrated circuit device of Claim 3,~~ An integrated circuit device, comprising:

an integrated circuit chip having a clock driver therein that supports generation of a plurality of output clock signals having different frequencies in a range between 1 and 1/N times a frequency of an internal clock signal and full-period programmable skew characteristics, where N is a positive integer greater than one;

wherein the clock driver comprises an internal clock signal generator selected from the group consisting of a phase-locked loop (PLL) integrated circuit and a delay-locked loop (DLL) integrated circuit;

wherein the clock driver is configured to support generation of a divide-by-N clock signal having a full-period programmable skew characteristics that is stepped in NxM time units having a duration equal to 1/M times a period of the internal clock signal, where M is a positive integer greater than eight; and

wherein the clock driver comprises:

a divide-by-N clock generator **[[that is]]** responsive to a first skew signal; and

a synchronization unit **[[that is]]** electrically coupled to an output of said divide-by-N clock generator circuit and responsive to the first skew signal.

7. (Currently amended) ~~The integrated circuit device of Claim 3,~~ An integrated circuit device, comprising:

an integrated circuit chip having a clock driver therein that supports generation of a plurality of output clock signals having different frequencies in a range between 1 and 1/N times a frequency of an internal clock signal and full-period programmable skew characteristics, where N is a positive integer greater than one;

wherein the clock driver comprises an internal clock signal generator selected from the group consisting of a phase-locked loop (PLL) integrated circuit and a delay-locked loop (DLL) integrated circuit;

wherein the clock driver is configured to support generation of a divide-by-N clock signal having a full-period programmable skew characteristics that is stepped in NxM time units having a duration equal to 1/M times a period of the internal clock signal, where M is a positive integer greater than eight; and

wherein the clock driver comprises:

a divide-by-N clock generator circuit **[[that is]]** configured to generate N divide-by-N clock signals that have the same frequency but are phase shifted relative to each other, in response to a first skew signal;

a one-of-N select circuit **[[that is]]** configured to select one of the N divide-by-N clock signals in response to a time unit position signal; and

a synchronization unit **[[that is]]** electrically coupled to an output of said one-of-N select circuit and **[[is]]** synchronized to the first skew signal.

8. (Currently amended) The integrated circuit device of Claim 7, wherein the clock driver further comprises a phase interpolator circuit **[[that is]]** configured to generate the first skew signal.

9. (Currently amended) The integrated circuit device of Claim 7, wherein the clock driver further comprises:

a delay chain and phase interpolator circuit [[that is]] configured to generate the first skew signal in response to a fine skew select signal.

10. (Currently amended) The integrated circuit device of Claim 9, wherein the clock driver further comprises:

a multiplexer [[that is]] configured to receive a plurality of skew signals from the internal clock signal generator ~~voltage-controlled oscillator~~ and pass a selected one of the plurality of skew signals to said delay chain and phase interpolator circuit in response to a coarse skew select signal.

11. (Currently amended) ~~The integrated circuit device of Claim 3,~~ An integrated circuit device, comprising:

an integrated circuit chip having a clock driver therein that supports generation of a plurality of output clock signals having different frequencies in a range between 1 and 1/N times a frequency of an internal clock signal and full-period programmable skew characteristics, where N is a positive integer greater than one;

wherein the clock driver comprises an internal clock signal generator selected from the group consisting of a phase-locked loop (PLL) integrated circuit and a delay-locked loop (DLL) integrated circuit;

wherein the clock driver is configured to support generation of a divide-by-N clock signal having a full-period programmable skew characteristics that is stepped in NxM time units having a duration equal to 1/M times a period of the internal clock signal, where M is a positive integer greater than eight; and

wherein the clock driver comprises:

a divide-by-N clock generator circuit [[that is]] configured to generate N divide-by-N clock signals that have the same frequency but are phase shifted relative to each other, in response to a first skew signal having a frequency equal to the frequency of the internal clock signal; and

a one-of-N select circuit [[that is]] configured to select one of the N divide-by-N clock signals in response to a time unit position signal.

12. (Currently amended) An integrated circuit chip, comprising:

a locked loop integrated circuit **[[that is]]** configured to generate a plurality of internal clock signals that are skewed in time relative to each but have the same first frequency;

a skew signal select circuit **[[that is]]** configured to generate a selected skew signal **[[that is]]** derived from at least one of the plurality of internal clock signals;

a divide-by-N clock generator circuit **[[that is]]** configured to generate a plurality of divide-by-N clock signals that have the same frequency but are phase shifted relative to each other in increments of 360°/N, in response to the selected skew signal, where N is a positive integer greater than one;

a synchronization unit **[[that is]]** configured to synchronize a selected one of the plurality of divide-by-N clock signals to the selected skew signal; and

an output buffer **[[that is]]** configured to drive an off-chip load with a divide-by-N output clock signal having a full-period skew characteristic, in response to a synchronized divide-by-N clock signal derived from said synchronization unit.

13. (Original) The integrated circuit chip of Claim 12, wherein the locked loop integrated circuit is selected from the group consisting of a delay-locked loop (DLL) integrated circuit and a phase-locked loop (PLL) integrated circuit.

14. (Currently amended) The integrated circuit chip of Claim 12, wherein the output buffer has a pair of differential outputs that are configured to generate a pair of differential divide-by-N output clock signals having full-period skew characteristics.

15. (Currently amended) The integrated circuit chip of Claim 12, wherein the skew signal select circuit comprises:

a multiplexer [[that is]] configured to receive the plurality of internal clock signals; and

a delay chain and phase interpolator circuit [[that is]] electrically coupled to an output of said multiplexer and [[is]] configured to generate the selected skew signal.

16. (Currently amended) The integrated circuit chip of Claim 12, wherein the skew signal select circuit comprises:

a multiplexer [[that is]] configured to receive the plurality of internal clock signals; and

a phase interpolator circuit [[that is]] electrically coupled to a pair of outputs of said multiplexer and [[is]] configured to generate the selected skew signal.

17. (Currently amended) The integrated circuit chip of Claim 12, wherein said divide-by-N clock generator comprises a one-of-N select circuit [[that is]] configured to select one of the plurality of divide-by-N clock signals, in response to a time unit position signal.

18. (Original) The integrated circuit chip of Claim 12, wherein said divide-by-N clock generator circuit is responsive to a multi-bit divide signal.

19. (Original) A method of generating a clock signal having a full-period programmable skew characteristic, comprising the steps of:

generating a plurality of internal clock signals that have equivalent frequencies, but are phase shifted relative to each other;

selecting at least one of the plurality of internal clock signals, in response to a coarse skew select signal;

generating a selected skew signal from the at least one selected plurality of internal clock signals;

generating a plurality of divide-by-N clock signals of equal frequency that are phase shifted relative to each other in increments of 360°/N, in response to the selected skew signal, where N is a positive integer greater than one;

selecting one of the plurality of divide-by-N clock signals, in response to a time unit position signal; and

synchronizing the selected one of the plurality of divide-by-N clock signals to the selected skew signal.

20. (Original) The method of Claim 19, further comprising the step of generating a pair of differential divide-by-N output clock signals from the synchronized divide-by-N clock signal.

21. (Currently amended) A method of operating an integrated clock driver circuit, comprising the step of:

generating a plurality of divide-by-N clock signals of equal frequency that are phase shifted relative to each other in increments of 360°/N, in response to a skew signal, where N is a positive integer greater than one;

selecting one of the plurality of divide-by-N clock signals, in response to a time unit position signal;

synchronizing the selected one of the plurality of divide-by-N clock signals to the **[[selected]]** skew signal; and

outputting the synchronized divide-by-N clock signal through an output buffer.

22. (Original) An integrated clock driver circuit, comprising:

means for generating a skew signal having full-period skew characteristic;

means responsive to the skew signal for generating N divide-by-N clock signals that are phase-shifted relative to each other in increments of 360°/N and have partial-period skew characteristics, where N is a positive integer greater than one; and

means for generating an output clock signal by selecting one of the N divide-by-N clock signals according to a desired full-period skew characteristic.

Claims 23-24 (Canceled).